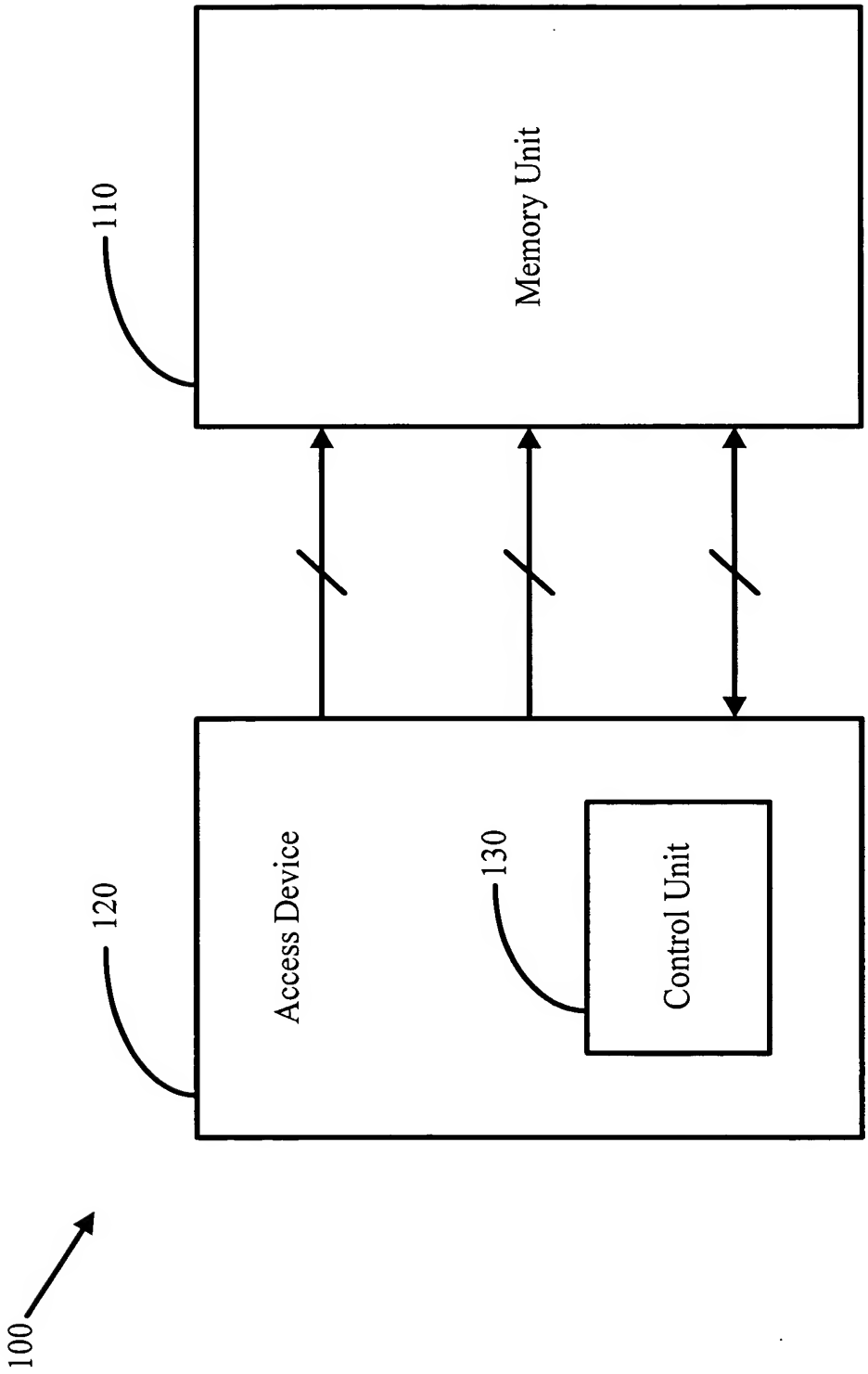

Figure 1

OIPE JC102 PATENT & TRADEMARK OFFICE JAN 13 2004

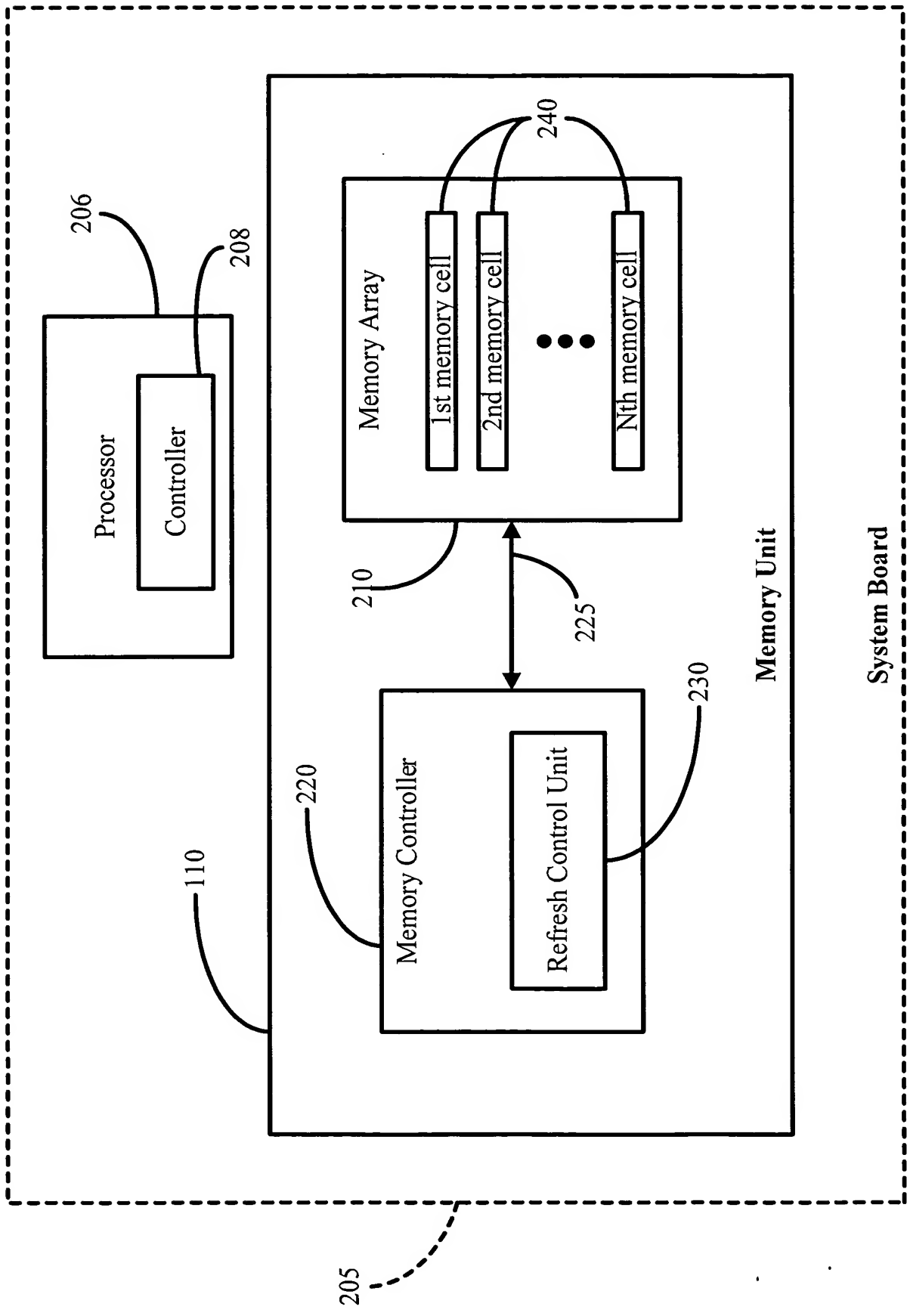
205
System Board
Memory Unit
110
Memory Controller
220
Refresh Control Unit
230
225
Memory Array
210
1st memory cell
2nd memory cell
Nth memory cell
240
Processor
Controller
206
208

Figure 2

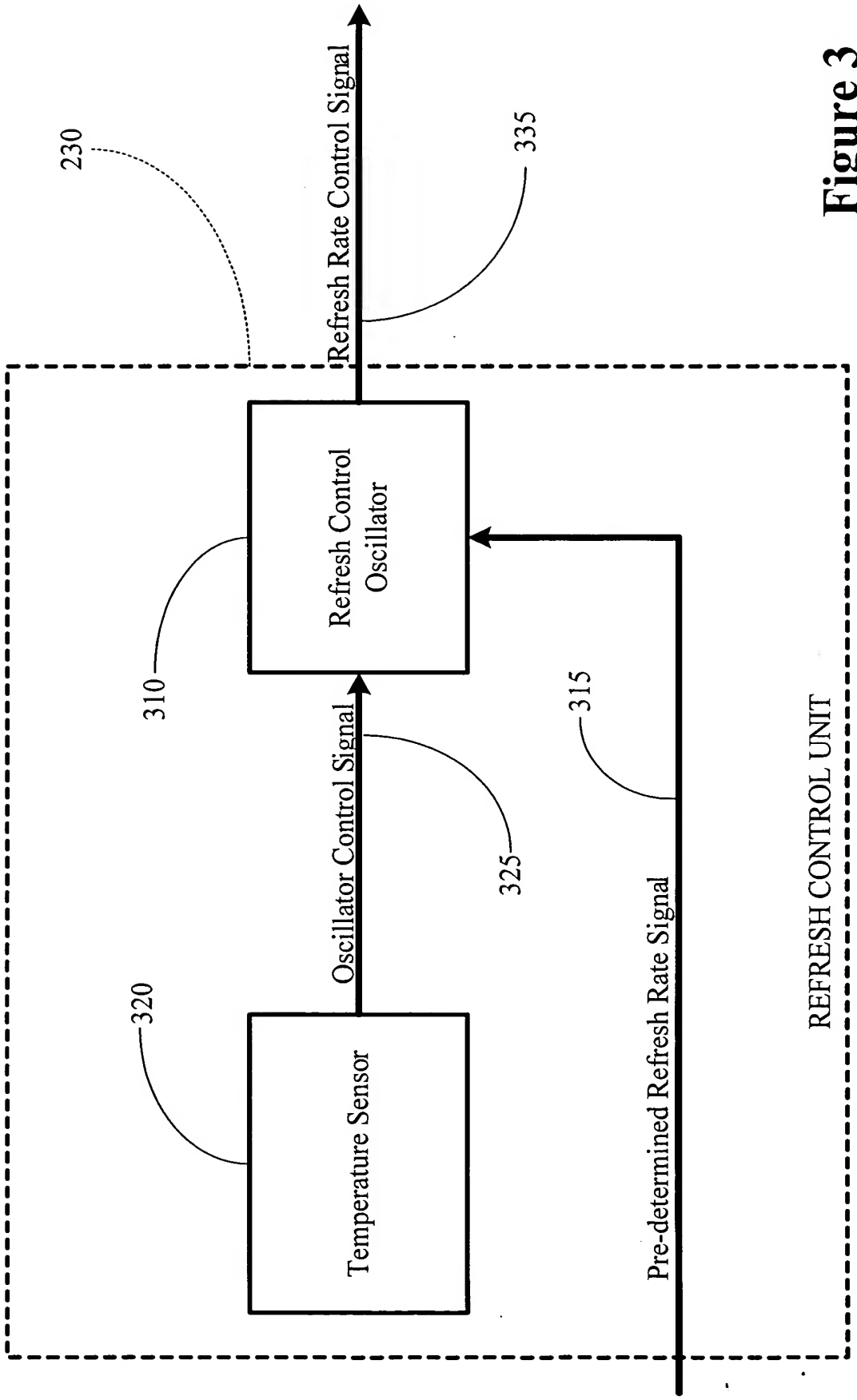
230
Refresh Rate Control Signal
335
Refresh Control Oscillator
310
Oscillator Control Signal
325
315
320
Temperature Sensor
Pre-determined Refresh Rate Signal
REFRESH CONTROL UNIT

Figure 3

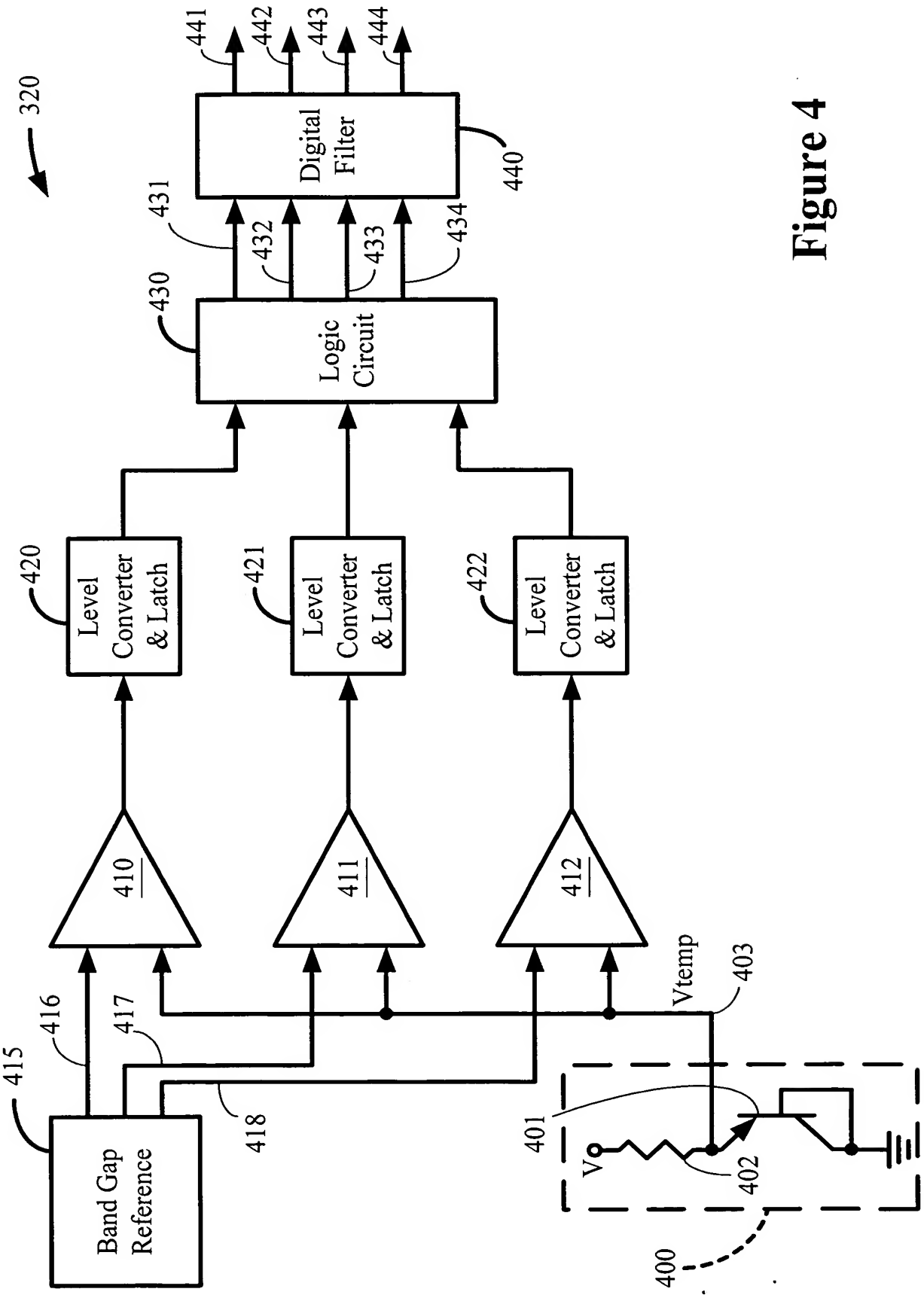
320
441
442
443
444
Digital Filter
440
431
432
433
434
430
Logic Circuit
420
421
422
Level Converter & Latch
Level Converter & Latch
Level Converter & Latch
410
411
412
415
416
417
418
Band Gap Reference
Vtemp
403
401
V
402
400

Figure 4

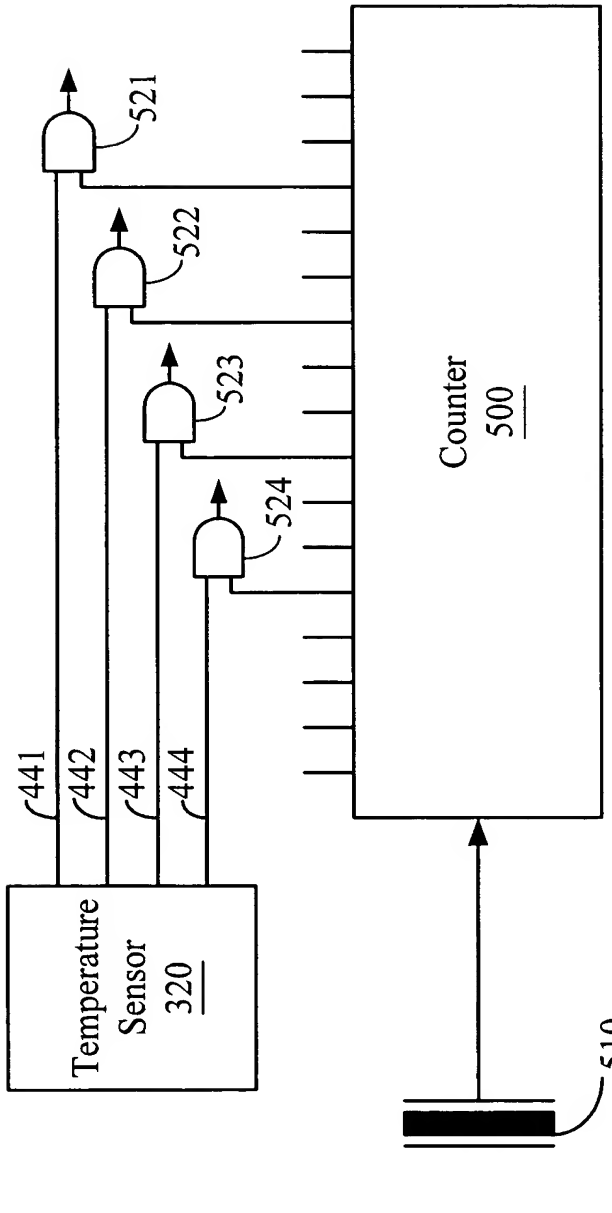
Temperature Sensor 320
441
442
443
444
521
522
523
524
Counter 500
510
310

Figure 5

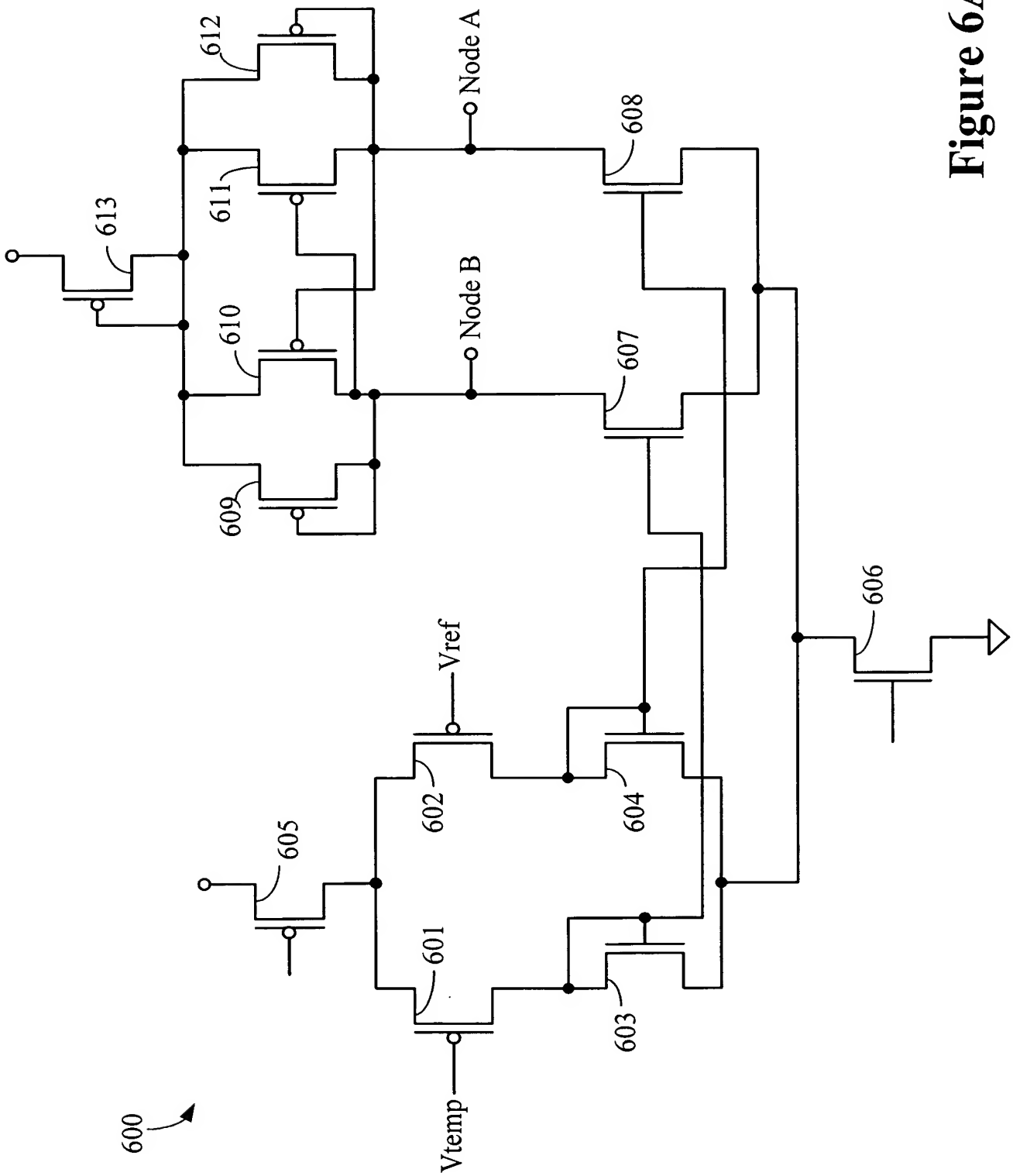
600
Vtemp
601
602
603
604
605
606
607
608
609
610
611
612
613
Node A
Node B
Vref

Figure 6A

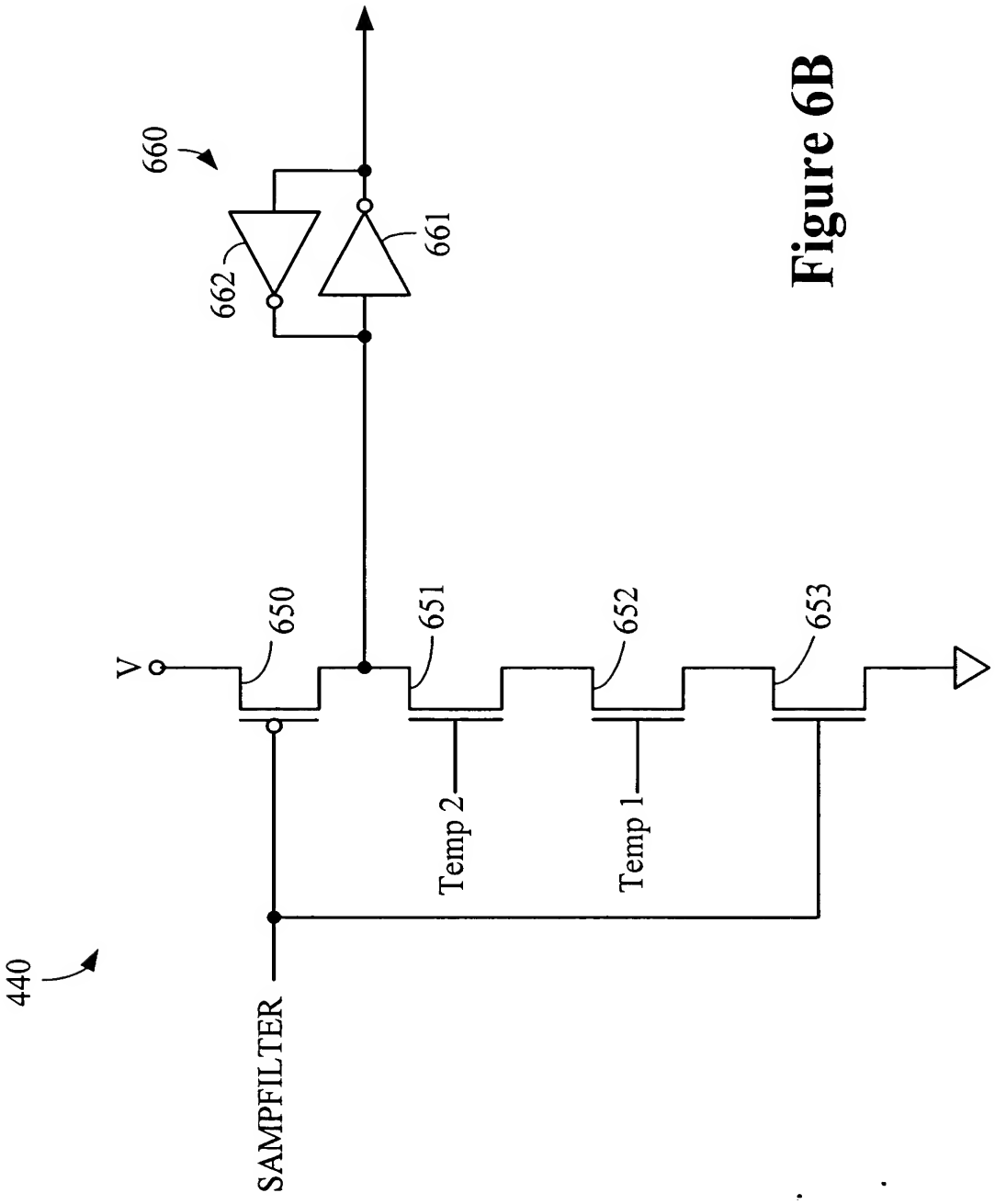

Figure 6B

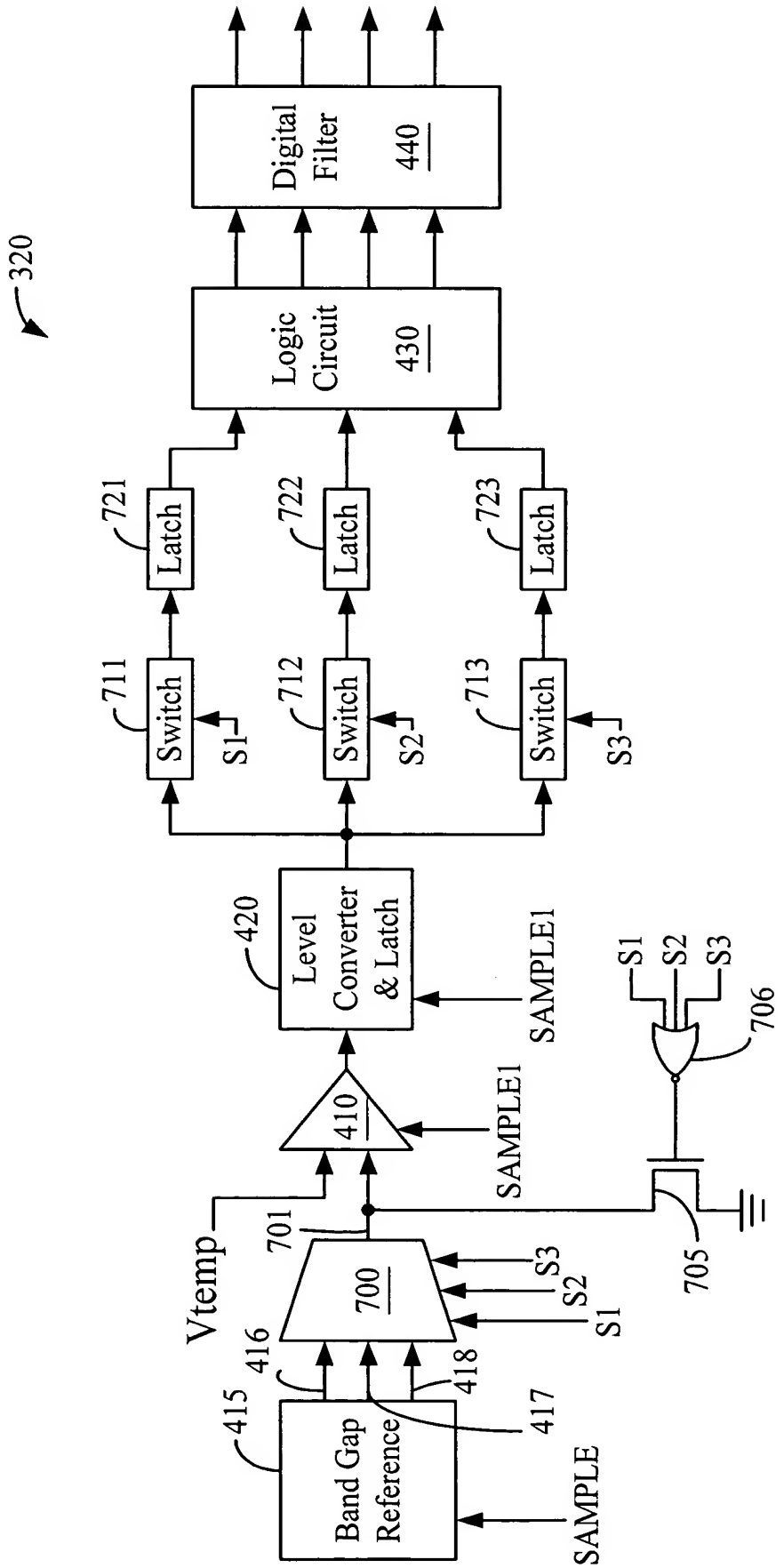
320
Digital Filter
440
Logic Circuit
430
721
Latch
722
Latch
723
Latch
711
Switch
712
Switch
713
Switch
S1
S2
S3
420
Level Converter & Latch
SAMPLE1
SAMPLE1
410
Vtemp
701
700
S3
S2
S1
416
418
415
417
Band Gap Reference
SAMPLE
S1
S2
S3
706
705

Figure 7

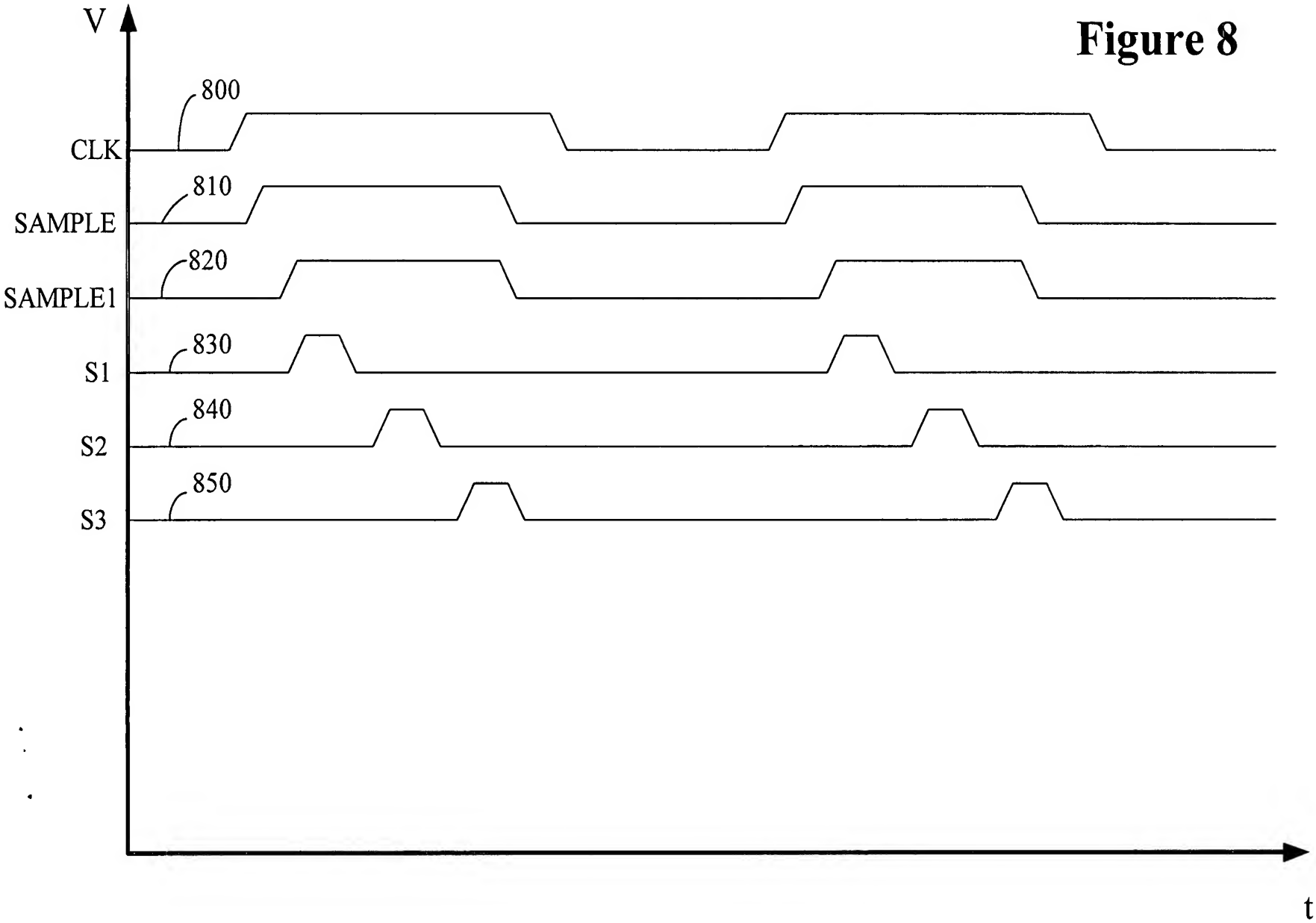

Figure 8